Notice of References Cited	Application/Control No. 10/050,793	Applicant(s)/Patent Under Reexamination EBINA, AKIHIKO	
	Examiner Thomas L Dickey	Art Unit 2826	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
	A	US-6268630 B1	07-2001	Schwank et al.	257/347
	B	US-			
	C	US-			
	D	US-			
	E	US-			
	F	US-			
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	Silicon Processing for the VLSI Era, Wolf, Stanley, Lattice Press, 1990. Volume II. Pages 557-558.
	V	SOI bipolar-MOS merged transistors for BiCMOS application; Zheng et al., Electronics Letters, Volume 35 Issue 14, 8 July 1999 Pages 1203 -1204
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.